Author: mgr inż. Mateusz Kuc

Abstract

Topic: "Low power LDPC code decoder implemented in FPGA structure "

Technological development made it possible to implement extensive digital systems in the form of specialized integrated circuits. One example of such systems are LDPC decoders, which are becoming more and more popular. They are used in various types of data transmission systems, among which you can find more and more systems implemented in mobile devices. Therefore, it is extremely important to look for low power LDPC decoders that will ensure longer operation of the electronic device without the need to replace the power source or frequently recharge the batteries. The search for such solutions became the subject of the research presented in the doctoral dissertation.

The essence of the work boiled down to the search for an low power LDPC decoder architecture that would significantly reduce energy losses while maintaining the corrective properties of the solutions used. Various types of circuit concepts were considered, among which special attention was paid to the GALS type. The specificity of the LDPC code decoding process, however, comes down to the sequential execution of calculations, which makes it difficult to look for significant energy benefits in the use of asynchronous data exchange mechanisms and local lowering of the clock frequency. In this situation, the search was focused on solutions in which subsequent computational modules are activated, and the calculation process is related to the sequential unblocking of the local clock signal. The result of the work related to numerous experiments is the proposed decoder architecture, called by analogy to network solutions the "Token Ring" architecture. The specificity of the hardware solution lies in the sequential "chip shift" that activates local clock signals in subsequent computational modules. An important aspect of the search are also numerous solutions aimed at effective technological reflection of computational algorithms in the hardware resources of the array--type FPGA circuits.

An important element of the work was to examine the relationship between the design assumptions, parameters of the control matrix $\boldsymbol{H}$, and the features characterizing the LDPC decoder. This allowed to determine the dependencies on the basis of which design guidelines were formulated, allowing the implementation of an low power LDPC decoder, meeting the requirements specified in the design assumptions.

The research methodology presented in the paper can be successfully used to analyze any parameters of the $\boldsymbol{H}$ control matrices and design parameters aimed at determining their relationship with the features of the LDPC decoder.

The presented solutions can be used in engineering practice, thus allowing to obtain low power electronic devices with built-in LDPC decoders.