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Description of the Doctoral Dissertation

The doctoral dissertation addresses **Multithreaded Selective Execution of Control Programs in Programmable Logic Controllers (PLCs)** using multicore processor architectures.

The main objective of the dissertation is to develop a hardware-software solution enabling efficient, predictable, and deterministic execution of control programs on multicore processors. The research investigates conventional hardware and software-based synchronization mechanisms as well as inter-processor interrupt-driven approaches. Particular attention is given to synchronization overhead, predictability, and deterministic execution behavior.

A dedicated hardware-based semaphore mechanism is developed to synchronize concurrently executed program fragments. The dissertation also proposes a **stalling-based synchronization mechanism**, which is evaluated against conventional and interrupt-driven synchronization approaches.

An important contribution of the dissertation is the development of a dependency-aware LLVM compiler mechanism operating at the middle-end level. The mechanism analyzes data and computational dependencies in PLC programs represented in LLVM IR, automatically partitions the program into fragments suitable for concurrent execution, assigns the fragments to the available processor cores, and generates the required synchronization operations.

The proposed solution enables the computational capabilities of multicore architectures to be exploited without requiring modifications to the existing PLC programming model. By implementing the mechanisms responsible for concurrent execution at the compiler level, the approach allows compatibility with programming languages defined by the IEC 61131-3 standard to be maintained while exploiting the parallelism available in the underlying processor architecture.

The dissertation combines research in the areas of computer architecture, multicore systems, hardware synchronization, compiler technology, and PLC-based control systems.